CLAIMS

Claims 1-22 *(CANCELED)*

23. *(ORIGINAL)* A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

receiving an enabled first clock signal;

receiving one or more data processing instructions with a first portion of a pipeline subcircuit;

executing said one or more data processing instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

receiving an operation suspension instruction with said first pipeline subcircuit portion and in response thereto

asserting one or more control signals from said pipeline subcircuit, followed by disabling said first clock signal.

24. *(ORIGINAL)* The method of claim 23, wherein said receiving an operation suspension instruction with said first pipeline subcircuit portion comprises receiving a halt instruction.

25. *(ORIGINAL)* The method of claim 23, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of said one or more data processing instructions; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled

first clock signal.

26. *(ORIGINAL)* The method of claim 23, further comprising, prior to said asserting one or more control signals, completing executing one or more of said one or more data processing instructions which had been received prior to said receiving said operation suspension instruction.

27. *(ORIGINAL)* The method of claim 26, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing one or more of said one or more data processing instructions; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

28. *(ORIGINAL)* The method of claim 23, further comprising, following said receiving said operation suspension instruction and prior to said asserting one or more control signals, completing executing one or more of said one or more data processing instructions which had been received prior to said receiving said operation suspension instruction.

29. *(ORIGINAL)* The method of claim 23, further comprising detecting an occurrence of a combination of respective states of one or more interrupt signals and in response thereto re-enabling said first clock signal.

30. *(ORIGINAL)* The method of claim 29, further comprising:

advancing one or more further data processing instructions into said first pipeline subcircuit portion; and

executing said one or more further data processing instructions with said second pipeline subcircuit portion in response to said re-enabled first clock signal.

31. *(ORIGINAL)* The method of claim 23, further comprising asserting a status signal indicative of said disabling of said first clock signal.

32. *(ORIGINAL)* The method of claim 31, further comprising, following said asserting of said one or more control signals, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said asserting of said status signal, and wherein said asserting a status signal indicative of said disabling of said first clock signal comprises asserting said status signal following an indication that said coprocessor operating status is in a selected state.

33. *(ORIGINAL)* The method of claim 23, further comprising, following said asserting of said one or more control signals, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said disabling of said first clock signal, and wherein said disabling said first clock signal comprises disabling said first clock signal following an indication that said coprocessor operating status is in a selected state.

34. *(ORIGINAL)* The method of claim 23, further comprising:

generating a second clock signal; and

maintaining said second clock signal in an enabled state substantially independently of said disabling of said first clock signal.

35. *(ORIGINAL)* A method for suspending operation of a pipelined data processor to reduce power consumption, comprising:

receiving an enabled first clock signal;

receiving one or more data processing instructions with a first portion of a pipeline subcircuit;

executing said one or more data processing instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal; and

receiving an operation suspension instruction with said first pipeline subcircuit portion and in response thereto

asserting one or more control signals from said first pipeline subcircuit portion, followed by

disabling said first clock signal.

36. *(ORIGINAL)* The method of claim 35, wherein said receiving an operation suspension instruction with said first pipeline subcircuit portion comprises receiving a halt instruction.

37. *(ORIGINAL)* The method of claim 35, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of said one or more data processing instructions; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

38. *(ORIGINAL)* The method of claim 35, further comprising, prior to said asserting one or more control signals, completing executing one or more of said one or more data processing instructions which had been received prior to said receiving said operation suspension

instruction.

39. *(ORIGINAL)* The method of claim 38, further comprising:

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing one or more of said one or more data processing instructions; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

40. *(ORIGINAL)* The method of claim 35, further comprising, following said receiving said operation suspension instruction and prior to said asserting one or more control signals, completing executing one or more of said one or more data processing instructions which had been received prior to said receiving said operation suspension instruction.

41. *(ORIGINAL)* The method of claim 35, further comprising detecting an occurrence of a combination of respective states of one or more interrupt signals and in response thereto re-enabling said first clock signal.

42. *(ORIGINAL)* The method of claim 41, further comprising:

advancing one or more further data processing instructions into said first pipeline subcircuit portion; and

executing said one or more further data processing instructions with said second pipeline subcircuit portion in response to said re-enabled first clock signal.

43. *(ORIGINAL)* The method of claim 35, further comprising asserting a status signal indicative of said disabling of said first clock signal.

44. *(ORIGINAL)* The method of claim 43, further comprising, following said asserting of said one or more control signals, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said asserting of said status signal, and wherein said asserting a status signal indicative of said disabling of said first clock signal comprises asserting said status signal following an indication that said coprocessor operating status is in a selected state.

45. *(ORIGINAL)* The method of claim 35, further comprising, following said asserting of said one or more control signals, monitoring an operating status of a coprocessor associated with said pipeline subcircuit prior to said disabling of said first clock signal, and wherein said disabling said first clock signal comprises disabling said first clock signal following an indication that said coprocessor operating status is in a selected state.

46. *(ORIGINAL)* The method of claim 35, further comprising:

generating a second clock signal; and

maintaining said second clock signal in an enabled state substantially independently of said disabling of said first clock signal.